Central™
Semiconductor Corp.

PROCESS CP229

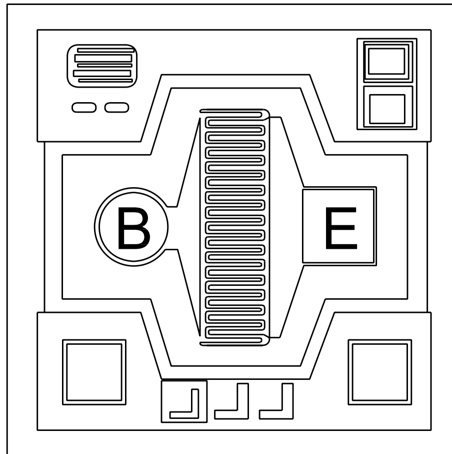
Small Signal Transistors

NPN - RF Transistor Chip

PROCESS DETAILS

Process	EPITAXIAL PLANAR
Die Size	21.7 x 21.7 MILS
Die Thickness	8.7 MILS
Base Bonding Pad Area	3.2 MILS Diameter
Emitter Bonding Pad Area	3.4 x 3.4 MILS
Top Side Metalization	Al - 10,000Å
Back Side Metalization	Au - 10,000Å

GEOMETRY



BACKSIDE COLLECTOR R0

GROSS DIE PER 4 INCH WAFER
17,000

PRINCIPAL DEVICE TYPES
2N5109

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R0 (23- September 2005)